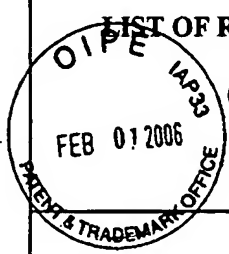


<div style="text-align: center;"> LIST OF REFERENCES CITED BY APPLICANT Form PTO-1449 <i>(Use several sheets if necessary)</i> </div> <div style="text-align: center; margin-top: 10px;"> Sheet 1 of 2 </div>	ATTY. DOCKET NO.: 4717-10400	APPLICATION NO.: 10/800,252
	APPLICANT: Fabrice LETERTRE et al.	
	FILING DATE: March 11, 2004	GROUP: 1734



U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	CITE NO.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
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MAD	AB	5,863,830	1/1999	Bruei et al.	438	478	
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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
MAD	AU	EP 0 106 566 B1	11/1989	Europe	—	—	X	
MAD	AV	EP 0 977 252 A1	2/2000	Europe	—	—	X	
MAD	AW	FR 2811807 with English Abstract	1/2002	France	—	—	X	
MAD	AX	JP 10320851 with English Abstract	12/1998	Japan	—	—	X	
MAD	AY	JP 6229849 with English Abstract	8/1994	Japan	—	—	X	
MAD	AZ	JP 3106052 with English Abstract	5/1991	Japan	—	—	X	

LIST OF REFERENCES CITED BY APPLICANT Form PTO-1449 <i>(Use several sheets if necessary)</i> Sheet 2 of 2					ATTY. DOCKET NO.:		APPLICATION NO.:	
					4717-10400		10/800,252	
					APPLICANT:			
					Fabrice LETERTRE et al.			
					FILING DATE:		GROUP:	
					March 11, 2004		1734	
FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
MAO	BA	WO 02/05344 A1	1/2002	PCT	—	—	X	
MAO	BB	WO 03/081664 A2	10/2003	PCT	—	—	X	
NON-PATENT DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)								
MAO	BC	S. Kodama et al., XP-000935156 "Variable Threshold AlGaAs/InGaAs Heterostructure Field-Effect Transistors with Paired Gated Fabricated Using the Wafer-Bonding Technique", Vol. 241ga, p. 434-435 (19099)						
EXAMINER					DATE CONSIDERED			
Mark A. Osiele					4-10-06			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								